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10/605,015	09/01/2003	Chih-Chin Chang	ADTP0094USA	2014

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
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EXAMINER
ARENA, ANDREW OWENS

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,015	CHANG ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Stacked capacitor having parallel interdigitized structure for use in thin film transistor liquid crystal display.

2. The abstract of the disclosure is objected to because of minor spelling errors. Line 1 contains "structureincludes" and line 8 contains "anda", both should be two separate words. Correction is required.

Claim Objections

3. Claim 20 is objected to because of the following informalities: spelling mistakes. Line 2 contains "thecapacitance" which should be two separate words. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4, 12, and 14 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claims 4, 12, and 14 contain the recitation "silicon oxide layer (SiOx layer, where $0<x<2.0$)", which is indefinite because silicon oxide is known in the art to correspond to

the chemical formula SiO_2 (www.semiconductorglossary.com defines oxide in the context of silicon processing as SiO_2).

7. Claims 4, 12, and 14 contain the recitation "silicon nitride layer (SiNy layer, where 0<y<1.33)", which is indefinite because silicon nitride is known in the art to correspond to the chemical formula Si_3N_4 (www.semiconductorglossary.com defines nitride in the context of silicon processing as Si_3N_4).

8. Claims 4, 12, and 14 contain limitations in parentheses. It is unclear weather applicant intends subject matter contained in the parentheses to be a limitation of the claim, or supplemental information. Applicant should keep claimed subject matter outside of parentheses.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Burkhardt et al. (US 6,259,149), hereinafter Burkhardt.

11. Regarding claim 1, Burkhardt discloses (Fig 6) a capacitor structure (col 6 ln 53) comprising:

a substrate (102+106; col 6 ln 54-56);

a first conductive layer (112; col 6 ln 57-62) disposed on the substrate;

a first insulating layer (116; col 6 ln 64) disposed on the first conductive layer;

a second conductive layer (118; col 6 ln 67) disposed on portions of the first insulating layer;

a second insulating layer (120; col 7 ln 3) disposed on portions of the second conductive layer and the first insulating layer;

a third conductive layer (122; col 7 ln 4-5) disposed on portions of the second insulating layer and electrically connecting to the first conductive layer (col 7 ln 6-7) through at least one first contact hole (vertical portion of 112 taken to be in a contact hole), the first contact hole being adjacent to the second conductive layer (vertical portion of 112 is adjacent to 118 by way of 120);

a third insulating layer (124; col 7 ln 7-8) disposed on the third conductive layer and the second insulating layer; and

a fourth conductive layer (126; col 7 ln 9) disposed on the third insulating layer and electrically connecting to the second conductive layer (col 7 ln 10) through at least one second contact hole (114 taken to be in a contact hole) and a fifth conductive layer (114; col 6 ln 60-63).

12. Regarding claim 3, Burkhardt discloses the structure of claim 1, wherein the first conductive layer is a polysilicon layer (col 6 ln 57-62).

13. Claims 1, 2, 4-17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda et al. (US 5,182,661), hereinafter Ikeda.

14. Regarding claim 1, Ikeda discloses (Fig 4B) a capacitor structure comprising:

a substrate (40);

a first conductive layer (68) disposed on the substrate;

a first insulating layer (42; col 5 ln 13) disposed on the first conductive layer;

a second conductive layer (60) disposed on portions of the first insulating layer;

a second insulating layer (44) disposed on portions of the second conductive layer and the first insulating layer;

a third conductive layer (62) disposed on portions of the second insulating layer and electrically connecting to the first conductive layer (col 5 ln 30) through at least one first contact hole (64), the first contact hole being adjacent to the second conductive layer (64 adjacent to 60 by way of 44);

a third insulating layer (46) disposed on the third conductive layer and the second insulating layer; and

a fourth conductive layer (22; portion right of 66) disposed on the third insulating layer and electrically connecting to the second conductive layer (col 5 ln 33-37) through at least one second contact hole (66) and a fifth conductive layer (22; portion left of and inside of 66).

15. Regarding claim 2, Ikeda discloses (Fig 4B) the structure of claim 1 wherein the substrate comprises a glass substrate (40).

16. Regarding claim 4, Ikeda discloses the structure of claim 1 wherein the first insulating layer comprises a silicon oxide layer (col 5 ln 13-14). Silicon oxide has been taken to mean SiO_2.

17. Regarding claim 5, Ikeda discloses the structure of claim 1 wherein both of the second conductive layer and the third conductive layer comprise a metal layer (col 5 ln 15-16 and 22).

18. Regarding claim 6, Ikeda discloses the structure of claim 1 wherein the metal layer comprises a chrome layer (col 5 ln 15; the first entry under chrome is chromium, in The American Heritage® Concise Dictionary).

19. Regarding claim 7, Ikeda discloses the structure of claim 1 wherein the fifth conductive layer is disposed in the second contact hole (portion of 22 in 66) to electrically connect the fourth conductive (22) layer and the second conductive (60) layer (col 5 ln 33-35).

20. Regarding claim 8, Ikeda discloses the structure of claim 7 wherein the third conductive layer (62) and the fifth conductive layer (22) are not connected (Fig 4B).

21. Regarding claim 9, Ikeda discloses (Fig 4A and 4B) the structure of claim 7 wherein the substrate is an array substrate of a liquid crystal display (LCD), a pixel array area is included on a surface of the substrate (col 4 ln 60-63, col 5 ln 10-11), and the fourth conductive layer is electrically connected to a thin film transistor (TFT 14) in the pixel array area through the fifth conductive layer (22 to 34 by way of 36; col 3 ln 44-46).

22. Regarding claim 10, Ikeda discloses the structure of claim 9 wherein the capacitor structure is disposed in the pixel array area on the substrate to be used as a storage capacitor (Fig 4A and 4B; elements 60, 62 lie in 22, it is well known in the art that this figure represents a pixel array area).

23. Regarding claim 11, Ikeda discloses the structure of claim 1 wherein the substrate is an array substrate of a liquid crystal display (LCD), a periphery circuit area is included on a surface of the substrate, and the capacitor structure is disposed in the periphery circuit area on the substrate (Fig 4A; region not including TFT 14 regarded as periphery circuit area).

24. Regarding claim 12, Ikeda discloses the structure of claim 1 wherein the second insulating layer comprises a silicon nitride layer (col 5 ln 19). Silicon nitride has been taken to mean Si_3N_4.

25. Regarding claim 13, Ikeda discloses (Fig 4B) the structure of claim 1 wherein the first contact hole (64) is disposed in the first insulating layer (42) and the second insulating layer (44), and the first contact hole exposes portions of the first conducting layer (68; col 5 ln 29-33).

26. Regarding claim 14, Ikeda discloses the structure of claim 1 wherein the third insulating layer comprises a silicon nitride layer (col 5 ln 25-26). Silicon nitride has been taken to mean Si_3N_4.

27. Regarding claim 15, Ikeda discloses the structure of claim 1 wherein the fourth conductive layer comprises an indium tin oxide (ITO) layer (col 5 ln 10-11).

28. Regarding claim 16, Ikeda discloses the structure of claim 1 wherein the second contact hole (66) is disposed in the second insulating layer (44), and the second contact hole exposes portions of the second conductive layer (60; col 5 ln 35-37).

29. Regarding claim 17, Ikeda discloses the structure of claim 1 wherein the first conductive layer, the first insulating layer, and the second conductive layer form a first

capacitor; the second conductive layer, the second insulating layer, and the third conductive layer form a second capacitor; and the third conductive layer, the third insulating layer, and the fourth conductive layer form a third capacitor (this is all inherent in the structure of Fig 4B, there must be a capacitance between each pair of conductors spaced by an insulator).

30. Regarding claim 19, Ikeda discloses (Fig 4B) the structure of claim 17 utilizing multi-layered conductive layers as multi-layered electrode plates (68, 60, 62, 22) to form at least two stack capacitors (there must be a capacitance between each pair of conductors spaced by an insulator).

31. Regarding claim 20, Ikeda discloses the structure of claim 17 wherein the capacitance value of the capacitor is equal to the capacitance value of an equivalent capacitor including the first capacitor, the second capacitor, and the third capacitor connected in parallel with one another (inherent in the structure of Fig 4B).

Claim Rejections - 35 USC § 103

32. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda.

34. Regarding claim 18, Ikeda discloses (Fig 4B) the structure of claim 17 wherein the second conductive layer and the fourth conductive layer are used as one electrode of the capacitor, but does not disclose the polarity, and the second conductive layer and

the fourth conductive layer are electrically connected by the fifth conductive layer through the second contact hole; the first conductive layer and the third conductive layer are used as the other electrode of the capacitor, but does not disclose the polarity, and the first conductive layer and the third conductive layer are electrically connected through a first contact hole filled with the third conductive layer.

35. It is apparent that the capacitor can be connected such that a given electrode can have either polarity, depending on the polarities desired for other components of the TFT-LCD device. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to connect the capacitor with the polarities as claimed, since there is no obvious advantage of either particular choice.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven Loke
Primary Examiner